COMPUTER PROCESSOR ARCHITECTURE SELECTIVELY USING FINITE-STATE-MACHINE FOR CONTROL CODE EXECUTION

ABSTRACT OF THE DISCLOSURE

[37] A microprocessor architecture including a finite state machine in combination with a microcode instruction cache for executing microinstructions. Microinstructions which would normally result in small sequences of high-repetition looped operations are implemented in a finite state machine (FSM). The use of the FSM is more energy-efficient than looping instructions in a cache or register set. In addition, the flexibility of a cache, or other memory oriented approach, in executing microcode instructions is still available. A microinstruction is identified as an FSM operation (as opposed to a cache operation) by an ID tag. Other fields of the microinstruction can be used to identify the type of FSM circuitry to use, direct configuration of a FSM to implement the microinstruction, indicate that certain fields are to be implemented in one or more FSMs and/or in memory-oriented operations such as in a cache or register.

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